

Application/Control Number: 10/054,374

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1. (Currently amended) A system for three-dimensional packaging of platelets, comprising in combination:

a slotted file; and

a plurality of platelets which fit into the slotted file, wherein each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier, and wherein the platelets are stacked in the slotted file forming a three-dimensional integrated circuit package; and

epoxy sealing the plurality of platelets into the slotted file to form a three-dimensional integrated circuit package.

2. (Original) The system of Claim 1, wherein the slotted file has at least three walls.

3. (Original) The system of Claim 2, wherein the at least three walls are composed of silicon.

4. (Original) The system of Claim 2, wherein the slotted file has at least two side walls and at least one back wall.

5. (Original) The system of Claim 4, wherein the at least two side walls have been etched with a plurality of grooves.

6. (Original) The system of Claim 5, wherein a depth of the plurality of grooves is sufficient to hold each of the plurality of platelets.

7. (Original) The system of Claim 5, wherein a spacing between the plurality of grooves is determined based on a platelet thickness.

8. (Previously presented) The system of Claim 5, wherein the spacing between the plurality of grooves is determined based on a number of platelets in the three-dimensional integrated circuit package.

9. (Original) The system of Claim 5, wherein the spacing between the plurality of grooves is determined based on an allocated space limitation.

10. (Original) The system of Claim 4, wherein the at least one back wall is connected to an end of each of the at least two side walls to form a "U" shape.

11. (Original) The system of Claim 10, wherein the plurality of grooves on the at least two side walls face directly across from each other.

12. (Canceled).

13. (Previously presented) The system of Claim 1, wherein the chip carrier has a floor and a frame.

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14. (Original) The system of Claim 13, wherein the floor and the frame are composed of a ceramic material.

15. (Original) The system of Claim 13, wherein the floor protrudes past at least two edges of the frame forming flanges.

16. (Original) The system of Claim 15, wherein the flanges fit into the plurality of grooves in the at least two side walls of the slotted file.

17. (Previously presented) The system of Claim 13, wherein the floor includes the plurality of electrodes.

18. (Original) The system of Claim 17, wherein the semiconductor chip is placed face down on the floor contacting the plurality of electrodes.